AMENDMENTS TO THE SPECIFICATION

IN THE TITLE:

The title of the invention as been amended to read --DATA DRIVEN TYPE ~~INFORMATION PROCESSING~~ APPARATUS AND METHOD ~~OF CONTROLLING EXECUTION THEREOF~~ WITH ROUTER OPERATING AT A DIFFERENT TRANSFER RATE THAN SYSTEM TO ATTAIN HIGHER THROUGHPUT--.

IN THE SPECIFICATION:

The paragraph beginning on page 6, line 2, has been amended as follows:

Fig. 12 is a block diagram showing an example of use of the router. In the configuration shown in Fig. 12, a plurality of data driven type processors PEs shown in Fig. 11 are connected through a router 5. When none of the data driven type processors performs a process, an input data is output as it is through router 5. When a process proceeds in the order of processor PE1 → PE1 → ~~PE~~PE3→ PE2, the input data is first provided from router 5 → 5a to processor PE1, the data processed by processor PE1 is again input to processor PE1 through 5b → router 5 and again through 5a, the data processed by processor PE1 is fed to processor PE3 through 5b → router 5 → 5f, the data processed by processor PE3 is input to processor PE2 through ~~5r~~ 5e → router 5 → 5c, and the data processed by processor PE2 is output through 5d → router 5.

The paragraph beginning on page 17, line 19, has been amended as follows:

Fig. 4 is a block diagram of an M × N rate transfer router in accordance with a still further embodiment of the present invention. Here, M and N are natural numbers not smaller than 2, M and N may or may not be the same, and M may be larger than or smaller than N. The router shown in Fig. 4 has M inputs and N outputs, and formed by a M-input, 1-output junction unit 15a and a 1-input, N-output branching unit 15b. The junction unit 15a is formed by (M - 1) 2-input, 1-output junction units. The router provides M × N paths.

The paragraph beginning on page 17, line 32, has been amended as follows:

When the relation is (M < N), the transfer rate of the path 15c between junction unit 15a and branching unit 15b will be the total sum of the transfer rates of outputs OUT1 to OUTN. For example, when outputs OUT1 to OUTN all have the same transfer rate, the path 15c will have the ~~M-times~~N-times transfer rate. When the relation is (M = N), the transfer rate of the path 15c between junction unit 15a and branching unit 15b may be M times or N times.

The paragraph beginning on page 18, line 31, has been amended as follows:

For this purpose, a ~~relay~~ delay element 4f is provided in the C element. As already described, the time for processing or the delay in the logic unit or the operating unit is considerably longer than the time for processing or the delay in the C element or in the pipeline register. Therefore, when the delay element 4f

in the C element used in the data driven type processor is implemented by a serial connection of inverter circuits, the delay element would have ten to several tens of stages. Therefore, the number of stages of the series connected inverters in the delay element 4f of the C element in the router in accordance with the embodiments of the present invention can be readily reduced to 1/2, 1/4, 1/M or 1/N (where M and N are natural numbers) of the number of stages in the C element in the data driven type processor.